**Lecture #19 Worksheet, Answer Master**

**Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Classification/section: \_\_\_\_\_\_\_\_\_\_\_\_\_**

**Fill in blanks to answer questions below. Then email this sheet to your TA.**

1. **What it the purpose of the MIPS control unit?**

1. **What two bit-fields (i.e., group of bits) of the instruction go directly into the CPU? What are the names of the two bit-fields?**

1. **What three bit-fields go directly to the register block, and what physical hardware do they designate?**

1. **What six-bit field does the ALU control use?**

1. **The diagram on slide 7 shows that only three bits, for a total of 8 possible operations, are sent to the ALU, even though the ALU control block has eight inputs, which could be used to identify up to 256 ALU functions. Why are so many inputs used but so few possibilities included?**

1. **The Control Decoder decodes what bit field?**

1. **What does the Mem-to-Reg control line select?**

1. **What do the Mem Read and Mem Write lines do?**

1. **What does the ALU Source line do?**

1. **Study the value of the op code control signals (that is, 0 or 1), and what each value signifies to the ALU (slides 9 and 10).**
2. **Study the op code decoder diagram shown, and understand how different instructions can activate the same control line.**
3. **As a register-to-register instruction is processed (slides 14-17), how many control lines are activated? Count the two lines from the Op Code decoder to the ALU Control decoder as a single line.**

1. **With the same assumptions as in Question 12, how many lines are activated?**

1. **With the same assumptions as in 12 and 13, how many control lines are activated in a branch instruction?**

1. **When adding the jump control circuitry, how many MUX’s are included in the CPU design?**

1. **With the signal and data paths in an active jump instruction, how fast do you think that the jump is executed?**

1. **Complete exercise 1 and then check your answers on slide 24.**
2. **Explain the inefficiency of the single-cycle architecture (slides 25 and 26).**

1. **Explain the multicycle implementation approach.**

1. **What is the speed advantage for the multicycle implementation?**

1. **What else is saved?**

1. **One problem with the multicycle implementation is that during each clock cycle, only one-fifth of an instruction is completed—it takes 5 clock cycles to complete one instruction. Thus, partial results after each cycle before the last one must be preserved. Referring to slides 33 and 34, what data must be saved?**

1. **From slide 35, what new operations does the ALU have to perform?**
2. **Slide 37 shows the full multicycle implementation CPU, with all control functions included. Name any three of the new control lines that are added (above those on the single cycle CPU).**

1. **Although students do NOT need to memorize this CPU variant for the final test, they should study it so that the transition to the pipeline architecture will be more understandable.**
2. **Do Exercise 2 on slide 39 (use the diagram on slide 40), then check your answers on slide 41.**